All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of Claims 17-20 rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,235,600 to Chiang et al is requested based on the following remarks.

Applicant agrees that Chiang discloses a transistor having sidewall spacers. However, Chiang differs from Applicant's teaching in an important way. Referring to Fig. 5 of Chiang, the final form of the device has sidewall spacers but does not have a liner oxide layer overlying the polysilicon trace. All of the oxide layers 4, 6, 9 have been removed for the top surface of the gate 3. By comparison, Applicant's device, as shown in Figs. 7-9, has a liner oxide layer 50 overlying the polysilicon trace 56. This feature is described in the original Claim 17, line 5. The teachings of Chiang et al do not anticipate Applicant's device, as described in Claim 17, because an important feature is not included in Chiang. Therfore, Claim 17 should be in condition for allowance. Dependent Claims 18-20 represent patentably distinct, further limitations on Claim 17 and should also be in condition for allowance. Finally, Claims 21-28

include the above-described feature, are narrower constructions of Claim 17, and should be in condition for allowance.

Reconsideration of Claims 17-20 rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,235,600 to Chiang et al is requested based on the above remarks.

Applicants have reviewed the prior art made of record and not relied upon and agree with the Examiner that while the references are of general interest, they do not apply to the detailed Claims of the present invention.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner F. Erdem not find that the Claims are now Allowable that he call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,

Douglas R. Schnabel, Reg. No. 47,927

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please add the following Claims:

21. The method according to Claim 17 wherein said silicon nitride layer is formed by one of the group of: growing by thermal process and depositing by chemical vapor deposition.

22. A MOSFET device comprising:

an insulator layer overlying a semiconductor substrate;

polysilicon traces overlying said insulator layer wherein said polysilicon traces comprise transistor gates;

a liner oxide layer overlying said polysilicon traces;

silicon nitride spacers on sidewalls of said polysilicon traces and overlying said liner oxide layer wherein said silicon nitride spacers have an L-shaped profile; and

an interlevel dielectric layer overlying said polysilicon traces, said silicon nitride spacers, and said liner oxide layer.

23. The device according to Claim 22 wherein said liner oxide layer has a thickness of between about 50 Angstroms and 300 Angstroms.

24. The device according to Claim 22 wherein said interlevel dielectric layer comprises a combination material from the group of: TEOS undoped oxide, boron phosphosilicate glass (BPSG), undoped silicon dioxide, silicon nitride, and silicon oxynitride.

25. The method according to Claim 22 wherein said silicon nitride layer is formed by one of the group of: growing by thermal process and depositing by chemical vapor deposition.

26. A MOSFET device comprising:

an insulator layer overlying a semiconductor substrate;

polysilicon traces overlying said insulator layer wherein said polysilicon traces comprise transistor gates;

a liner oxide layer overlying said polysilicon traces;

silicon nitride spacers on sidewalls of said polysilicon traces and overlying said liner oxide layer wherein said silicon nitride spacers have an L-shaped profile and wherein said silicon nitride layer is formed by chemical vapor deposition; and

an interlevel dielectric layer overlying said polysilicon traces, said silicon nitride spacers, and said liner oxide layer.

27. The device according to Claim 26 wherein said liner oxide layer has a thickness of between about 50 Angstroms and 300 Angstroms.

28. The device according to Claim 26 wherein said interlevel dielectric layer comprises a combination material from the group of: TEOS undoped oxide, boron phosphosilicate glass (BPSG), undoped silicon dioxide, silicon nitride, and silicon oxynitride.